IDS 5922: Preparing for College Teaching
Demo Assessment Draft

BACKGROUND

Course Title: Computer Architecture

Description: This is an upper level undergraduate course for Computer Science & Engineering majors. Students must have previously taken undergrad level Computer Organization course before taking this course. The focus of this course is the principles of modern computer architecture. Students will know how to design better computing systems for specific applications as well as general purpose computers. Besides they will know the implications of Moore's Law in the advancement of computing technologies. Students will also gain hands-on knowledge on modern memory system design and the effect of cache hierarchy on computing performance in terms of cost, power and execution time.

LEARNING OUTCOMES

1. Students will be able to identify the limiting factors towards the development of faster but cheaper computers.
    - Bloom Level = Knowledge
    - Students will know what are the root causes that have slowed down the faster computer designs in the last several years.
2. Given several types of cache memory blocks and their bandwidths and costs, students will be able to place them in correct hierarchy and assign correct block size or word size for each of them.
    - Bloom Level = Applying
    - This learning outcome measures if students have necessary understanding of the cache hierarchy and the role of different level of caches in computer designs. They can apply their understanding of cache hierarchy to organize the caches in correct order and assign configurations to those cache blocks. I want to use a rubrics to evaluate the students' response to this question.
3. Given a very large matrix multiplication problem, students in several groups will be asked to design a computing architecture/platform. Students will put their argument to champion a computing platform that will win in terms of a given execution time. A reference architecture will be provided and each group will present their argument in favor of their own design in a gallery walk.
    - Bloom Level = Evaluating
    - This assessment aligns with the course objective that students will be able to design and appreciate an application specific architecture. This assessment will be authentic.

ASSESMENT MATERIALS

1. (True or False). Power wall limits the ability to scale a design to high-clock rate.
   Learning outcome: 1
2. Suppose you can utilize 4MB of SRAM1(BW 28.8Gb/sec) and 32MB of SRAM2 (BW 8Gb/sec) and unlimited DRAMs to design a cache hierarchy system for a 64 bit ISA. Use suitable organization in terms of cache serialization, size distribution, Bank allocation, nature of the cache (private/shared/spilit) of these memory.
   Learning outcome: 2
3. Use matrix size = 1000 for the below C implementation of matrix multiplication.

```
4. void init_matrix( double **matrix, int size )
5. {
6. int i, j;
7. for (i = 0; i < size; ++i) {
8.     for (j = 0; j < size; ++j) {
9.         matrix[ i ][ j ] = 1.0;
10.             }
11.          }
12. }
```

   Propose a parallel architecture to achieve best instruction per cycle (IPC) for this C code. Highlight the IPC calculation for your proposed arch. Develop a gem5 simulation model according your architecture configuration. Compare the IPC of your proposed arch. to the reference gem5 model provided in the course website. Discuss the possible reason/s why the IPC differs (if any) and present your observation to your peers.
   Learning outcome: 3

GRADING SCHEME

1. True or False: True
2. Students response can vary a lot for this question as the considerations for the organization can also vary a lot. This question will carry a total of 10 points divided into 4 categories.

	10 points	8 points	4 points	2 points
Cache serialization	SRAM1>SRAM2>DRAM	SRAM2>SRAM1>DRAM	NA	NA
Size Distribution	4MB -> 16MB -> 64MB	2 MB -> 4MB -> 16MB	4MB -> 32MB -> (any)	NA
Bank	1, 2, 1	1,1,1	NA	NA
Private/Shared	Private data/inst, shared, shared	Shared, shared, shared	Split, Split, Shared	Shared, shared, split

Testing the students understanding of cache organization is the main objective of this question. Students who got best understanding will utilize SRAMs on the top level and DRAM at the lower level. And the cache size in the lower level will be multiple of the higher levels.

3. The group with close to the reference IPC will get the highest points. Other than the IPC, student group have to explain the measured IPC to other group.